27. A memory device comprising:

a semiconductor substrate;

a first insulating layer on at least a memory cell area of said semiconductor substrate, wherein said first insulating layer defines a first plurality of openings leading to a respective plurality of impurity implanted regions;

a plurality of plugs, wherein each plug of said plurality of plugs is in one of said first plurality of openings;

a second insulating layer on said first insulating layer, wherein said second insulating layer defines a second plurality of openings at said memory cell area; and

a conductive material in each of said second plurality of openings; and

wherein said material in each of said second plurality of openings is electrically connected via one of said plurality of plugs to one of said plurality of impurity implanted regions.

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28. A semiconductor memory device, comprising:

a semiconductor substrate;

an impurity implanted region within said semiconductor substrate;

a first insulating layer on said semiconductor substrate, wherein said first insulating layer defines a contact opening leading to said impurity implanted region;

a plug inside said contact opening;

a second insulating layer on said first insulating layer and defining a second opening leading to said first insulating layer; and

an electrically conductive layer within said second opening and electrically connected via said plug to said impurity implanted region.

29. A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of impurity implanted regions within said semiconductor substrate;

a first insulating layer on said semiconductor substrate, wherein said first insulating layer defines a first plurality of openings, each leading to one of said plurality of impurity implanted regions;

a second insulating layer on said first insulating layer, wherein said second insulating layer defines a second plurality of openings, each corresponding to one of said first plurality of openings; and

a plurality of electrically conductive plugs, each in one of said first plurality of openings;

a conductive layer in each of said second plurality of openings and electrically connected via at least one of said plurality of electrically conductive plugs to at least one of said plurality of impurity implanted regions.

30. An electrical communication system for a memory device including a conductive material in a plurality of openings corresponding to a plurality of impure substrate regions, said system comprising a respective plurality of conductive plugs interposed between said plurality of impure substrate regions and said plurality of openings of said memory device.

31. The system of claim 30, wherein at least one of said plurality of conductive plugs is interposed between a source region and a portion of said conductive material in a respective opening of said plurality of openings.

32. The system of claim 30, wherein at least one of said plurality of conductive plugs is interposed between a drain region and a portion of said conductive material in a respective opening of said plurality of openings.

33. The system of claim 30, wherein a first plug of said plurality of conductive plugs is in electrical communication with a drain of a first transistor; and wherein a second plug of said plurality of conductive plugs is in electrical communication with a source of a second transistor.

34. A memory device portion, wherein said memory device includes a transistor gate, transistor source, and transistor drain, and said portion comprises:

a first oxide over said transistor gate and defining a first opening over at least a selection of said transistor source and said transistor drain;

a first conductive material within said first opening;

a second oxide over said first oxide and defining a second opening over said first conductive material; and

a second conductive material within said second opening.

35. The portion in claim 34, wherein said second conductive material directly contacts said first conductive material.

36. The portion in claim 34, wherein said first oxide is over at least apart of said transistor gate; and wherein said first oxide defines an opening over at least a part of said transistor drain.

37. The portion in claim 34, wherein said second oxide is over said transistor gate and defines said second opening over at least said selection of said transistor source and said transistor drain.

38. A semiconductor device, comprising:

a first conductive structure;

a second conductive structure lower than said first conductive structure;

a third conductive structure over said second conductive structure; and

a fourth conductive structure between said second conductive structure and said third conductive structure, wherein said fourth conductive structure is discrete from said third conductive structure;

wherein said first, second, third, and fourth conductive structures define at least a portion of circuitry of said semiconductor device.

39. The device in claim 38, wherein:

said first conductive structure is a transistor gate over a semiconductor substrate;

said second conductive structure is a source/drain impurity region of said semiconductor substrate; and

said fourth conductive structure is a plug.

40. The device in claim 39, further comprising a first insulative layer between said third conductive structure and said transistor gate, wherein said first insulative layer defines a first opening between said third conductive structure and said source/drain impurity region; and wherein said plug is within said first opening.

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41. The device in claim 40, further comprising a second insulative layer defining a second opening at least partially containing said third conductive structure.

42. An assembly for a conductive runner extending over and predominantly parallel to a semiconductor substrate, wherein said runner is flanked by a pair of conductive regions of said substrate, said assembly comprising:

a first insulator over said runner;

a second insulator over said first insulator and defining an opening; and

at least one conductive plug extending predominantly perpendicularly in relation to said semiconductor substrate, through said first insulator, and between at least one of said pair of conductive regions and said opening.

43. The assembly of claim 42, further comprising a conductive material within said opening.

44. The assembly of claim 43, wherein said plug directly contacts at least one of said pair of conductive regions.

45. Supplemental circuitry for a memory device including a wordline over a substrate and an impurity region of said substrate below and extending laterally from said wordline, said circuitry comprising:

a first conductor extending upward from said impurity region;

a first insulator co-extensive in height and extending laterally from around said first conductor;

a second insulator above and extending laterally from said first conductor, wherein said second insulator defines an opening, and wherein at least a portion of said opening is directly over at least a portion of said first conductor; and

a second conductor within said opening.

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46. A method of providing electrical communication with a transistor including a source/drain, said method comprising:

providing a conductor over said source/drain that extends upward and is laterally surrounded by a first layer of insulation;

providing a second layer of insulation over said first layer of insulation, wherein said second layer of insulation is higher than said conductor and exposes said conductor; and

allowing electrical communication with said source/drain only by way of said conductor.

47. The method in claim 46, wherein said step of providing a conductor comprises providing a plug.

48. A method of processing a device comprising a transistor, said method comprising:

providing a plug in electrical communication with said transistor;

providing a conductive material in electrical communication with said plug; and

providing an insulating layer lateral to said conductive material, wherein said step of providing an insulating layer occurs before said step of providing a conductive material.

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49. The method in claim 48, further comprising a step of providing a first insulating layer over said transistor; and wherein said step of providing an insulating layer lateral to said conductive material comprises providing a second insulating layer over said first insulating layer.

50. The method in claim 49, wherein said step of providing a conductive material is discrete from said step of providing a plug.